MULTI-RUN SELECTIVE PATTERN AND ETCH WAFER PROCESS

Abstract

A method for forming a semiconductor wafer comprising of applying a first patterned resist to at least one first predetermined region of a wafer where said at least one first predetermined region of said wafer are protected by said first patterned resist and a first remaining portion of said wafer is not protected by said first patterned resist; etching said first remaining portion of said wafer not protected by said first pattern resist; stripping the first pattern resist from said wafer; applying a second patterned resist to at least one second pre-determined region of said wafer where said at least one second predetermined region of said wafer are protected by a second patterned resist and a second remaining portion is not protected by said second patterned resist; etching said second remaining portion not protected by said second patterned resist; and stripping said second patterned resist from said wafer.